Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of Claims in the application.

Listing of Claims:

1. (Original): An array, comprising:

a plurality of three-color pixel elements, wherein each said three-color pixel element comprises:

a blue emitter disposed at a center of a square disposed at an origin of an X, Y coordinate system having a first, a second, a third, and a fourth quadrant, wherein said blue emitter is square-shaped;

a pair of red emitters spaced apart from said blue emitter and symmetrically disposed about said blue emitter in said second and said fourth quadrants, wherein said red emitters occupy a portion of said second and said fourth quadrants not occupied by said blue emitter, wherein said red emitters are generally square-shaped having truncated inwardly-facing corners forming edges parallel to sides of said blue emitter;

a pair of green emitters spaced apart from said blue emitter and symmetrically disposed about said blue emitter in said first and said third quadrants, wherein said green emitters occupy a portion of said first and said third quadrants not occupied by said blue emitter, wherein said green emitters are generally square-shaped having

truncated inwardly-facing corners forming edges parallel to said sides of said blue emitter;

wherein said array is repeated across a panel to complete a device with a desired matrix resolution forming a checker board of alternating said red emitters and said green emitters with said blue emitters distributed evenly across said device, wherein said blue emitters are at half resolution of said red emitters and said green emitters;

a first transistor for said blue emitter, a second transistor for said red emitter, and a third transistor for said green emitter, wherein said second and third transistors are grouped together at interstitial corners between said three-color pixel elements; and

column lines and row lines connecting to said first, second, and third transistors, wherein two of said column lines and two of said row lines are coupled to said second and third transistors in said interstitial corners.

2. (Original): The array of claim 1, further comprising associated structures connected to said first, second, and third transistors.

3. (Original): The array of claim 2, wherein said associated structures are capacitors.

4. (Original): An array, comprising:

a plurality of three-color pixel elements, wherein each said three-color pixel element comprises:

a blue emitter disposed at a center of a square disposed at an origin of an X, Y coordinate system having a first, a second, a third, and a fourth quadrant, wherein said blue emitter is square-shaped;

a pair of red emitters spaced apart from said blue emitter and symmetrically disposed about said blue emitter in said second and said fourth quadrants, wherein said red emitters occupy a portion of said second and said fourth quadrants not occupied by said blue emitter, wherein said red emitters are generally square-shaped having truncated inwardly-facing corners forming edges parallel to sides of said blue emitter;

a pair of green emitters spaced apart from said blue emitter and symmetrically disposed about said blue emitter in said first and said third quadrants, wherein said green emitters occupy a portion of said first and said third quadrants not occupied by said blue emitter, wherein said green emitters are generally square-shaped having truncated inwardly-facing corners forming edges parallel to said sides of said blue emitter; and

transistors coupled to said blue emitters, said red emitters, and said green emitters;

wherein said array is repeated across a panel to complete a device with a desired matrix resolution forming a checker board of alternating said red emitters and said green emitters with said blue emitters are distributed at a spatial frequency, wherein said blue emitters are at half resolution of said red emitters and said green emitters;

wherein said transistors for said red emitters and said green emitters are grouped together at interstitial corners between said three-color pixel elements;

column lines and row lines connecting to said transistors, wherein two of said column lines and two of said row lines are coupled to said transistors for said red emitters and said green emitters in said interstitial corners; and

wherein said transistors for said red emitters and said green emitters are disposed at locations in said array such that said transistors for said red emitters and said green emitters are disposed at said spatial frequency said blue emitters and are 180 degrees out of phase with said blue emitters, said transistors for said red emitters and said green emitters being sized to have a luminance value equal to a luminance value of said blue emitters.

5. (Original): The array of Claim 4, further comprising associated structures connected to said transistors.

6. (Original): The array of Claim 5, wherein said associated structures are capacitors.

7. (Original): The array of Claim 4, wherein a radiance value of said red emitters and said green emitters is substantially equal to a radiance value of said blue emitters.

8. (Original): The array of Claim 7, wherein said luminance value of said red emitters and said green emitters is substantially equal to said radiance value of said blue emitters is adjusted to provide a desired white color point.

9. (Original): An array, comprising:

a plurality of three-color pixel elements, wherein each said three-color pixel element comprises a blue emitter, a pair of red emitters, and a pair of green emitters arranged in a square design;

wherein said array is repeated across a panel to complete a device with a desired matrix resolution forming a checker board of alternating said red emitters and said green emitters with said blue emitters distributed evenly across said device, wherein said blue emitters are at half resolution of said red emitters and said green emitters;

a first transistor for said blue emitter, a second transistor for said red emitter, and a third transistor for said green emitter, wherein said second and third transistors are grouped together at interstitial corners between said three-color pixel elements; and

column lines and row lines connecting to said first, second, and third transistors, wherein two of said column lines and two of said row lines are coupled to said second and third transistors in said interstitial corners.

10. (Original): The array of claim 9, further comprising associated structures connected to said first, second, and third transistors.

11. (Original): The array of claim 10, wherein said associated structures are capacitors.

12. (Original): An array, comprising:

a plurality of three-color pixel elements, wherein each said three-color pixel element comprises a blue emitter, a pair of red emitters, and a pair of green emitters disposed in a square design, and transistors coupled to said blue emitters, said red emitters, and said green emitters;

wherein said array is repeated across a panel to complete a device with a desired matrix resolution forming a checker board of alternating said red emitters and said green emitters with said blue emitters are distributed at a spatial frequency, wherein said blue emitters are at half resolution of said red emitters and said green emitters;

wherein said transistors for said red emitters and said green emitters are grouped together at interstitial corners between said three-color pixel elements;

column lines and row lines connecting to said transistors, wherein two of said column lines and two of said row lines are coupled to said transistors for said red emitters and said green emitters in said interstitial corners; and

wherein said transistors for said red emitters and said green emitters are disposed at locations in said array such that said transistors for said red emitters and said green emitters are disposed at said spatial frequency of said blue emitters and are 180 degrees out of phase with said blue emitters, said transistors for said red emitters and said green emitters being sized to have a luminance value equal to a luminance value of said blue emitters.

13. (Original): The array of claim 12, further comprising associated structures connected to said transistors.

14. (Original): The array of claim 13, wherein said associated structures are capacitors.

15. (Original): The array of claim 12, wherein a radiance value of said red emitters and said green emitters is substantially equal to a radiance value of said blue emitters.

16. (Original): The array of claim 15, wherein said luminance value of said red emitters and said green emitters is substantially equal to said radiance value of said blue emitters is adjusted to provide a desired white color point.

17. (New): A pixel element for a display comprising:

a pair of red emitters disposed about an origin in a substantially rectangular coordinate system having four quadrants in a first pair of opposing quadrants;

a pair of green emitters disposed about said origin in said substantially said rectangular coordinate system in a second pair of opposing quadrants;

a blue emitter disposed at said origin of said rectangular coordinate system;

wherein each said red emitter and said green emitter is coupled to a transistor and such that each such transistor for said red and green emitter is substantially located in a interstitial corner of said substantially rectangular coordinate system.

18. (New): A display comprising substantially a plurality of three-color pixel elements, said three-color pixel element comprising:

a pair of red emitters;

a pair of green emitters; such that said red emitters and said green emitters substantially form a checkerboard pattern;

a blue emitter disposed at a center of said checkerboard pattern of said red emitters and green emitters; and

wherein each said red emitter and green emitter is connected to a transistor such that said transistors for said red and green emitters substantially form a dark spot in the interstitial corners between said pixel elements.

19. (New): The display of Claim 18 wherein each said emitter is independently addressable.

20. (New): The display of Claim 19 wherein each emitter is capable of being driven with a variable analog signal.

21. (New): The display of Claim 18 wherein said red emitters and said green emitters comprise a length approximately one half in the vertical axis to improve spatial addressability.

22. (New): A display comprising a plurality of a subpixel repeating group, said repeating group comprising blue subpixels, and at least a second colored subpixel and a third colored subpixel;

said second colored subpixels and said third colored subpixels are coupled to associated structures;

wherein said associated structures are grouped together upon said display such that said associated structures form dark spot regions such that the visibility of the pattern of said blue subpixels upon said display is decreased to the human viewer.

23. (New): The display of Claim 22 wherein said second colored subpixels are red subpixels and said third colored subpixels are green subpixels; and

wherein said red subpixels and said green subpixels comprise substantially a checkerboard pattern within said repeating group.

24. (New): The display of Claim 22 wherein said associated structures are transistors.

25. (New): The display of Claim 22 wherein said associated structures are capacitors.